

Fig. 1

09516408.021400

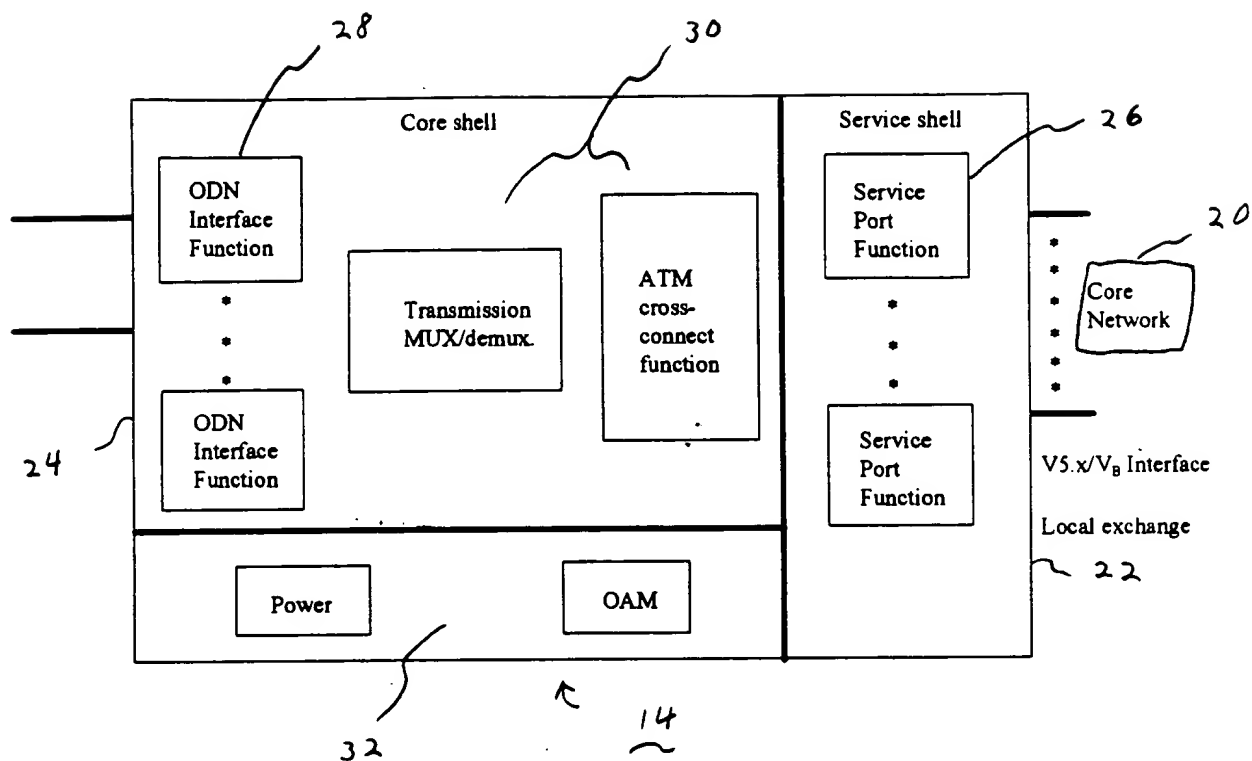


Fig. 2

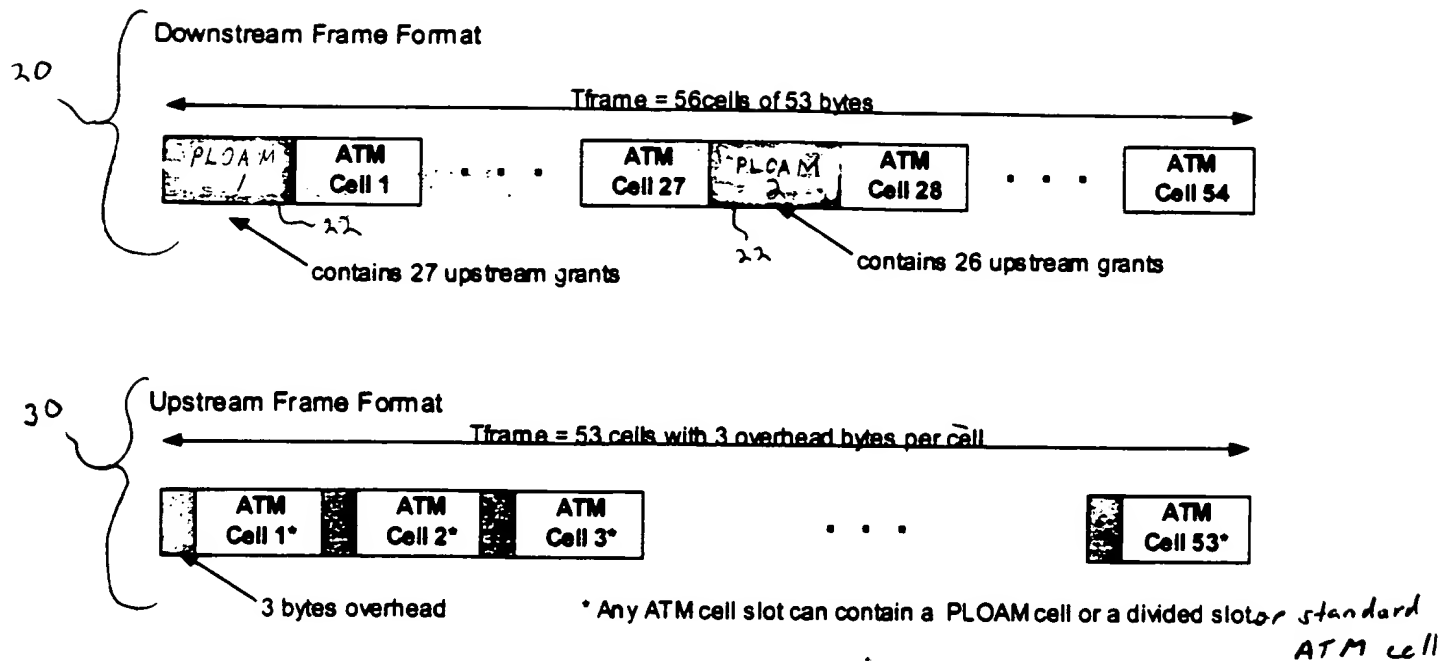


Fig. 3

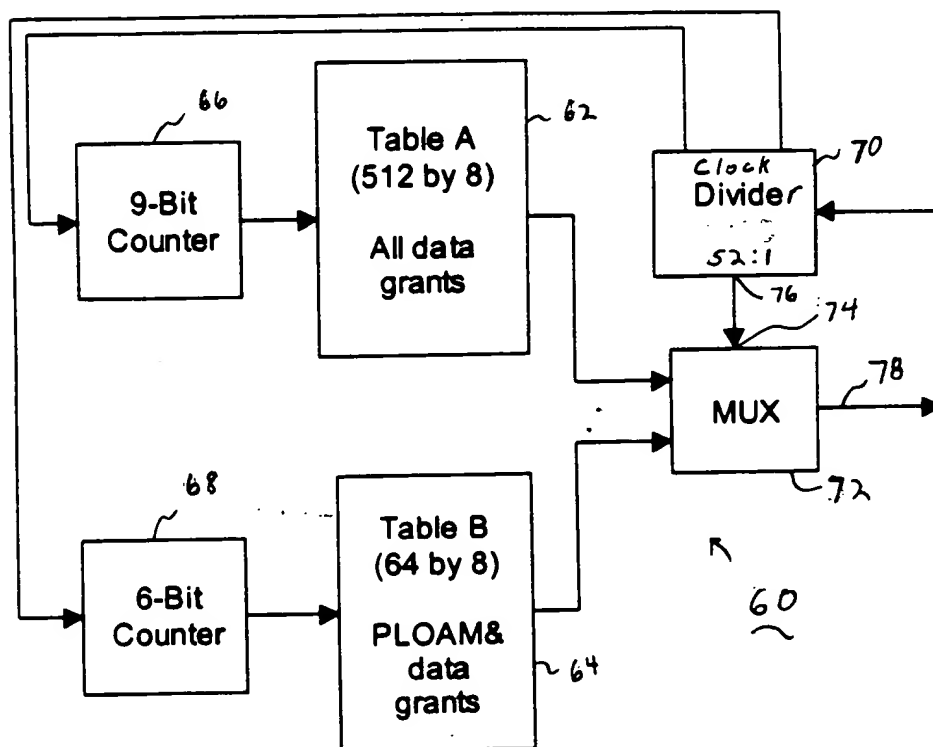


Fig 6

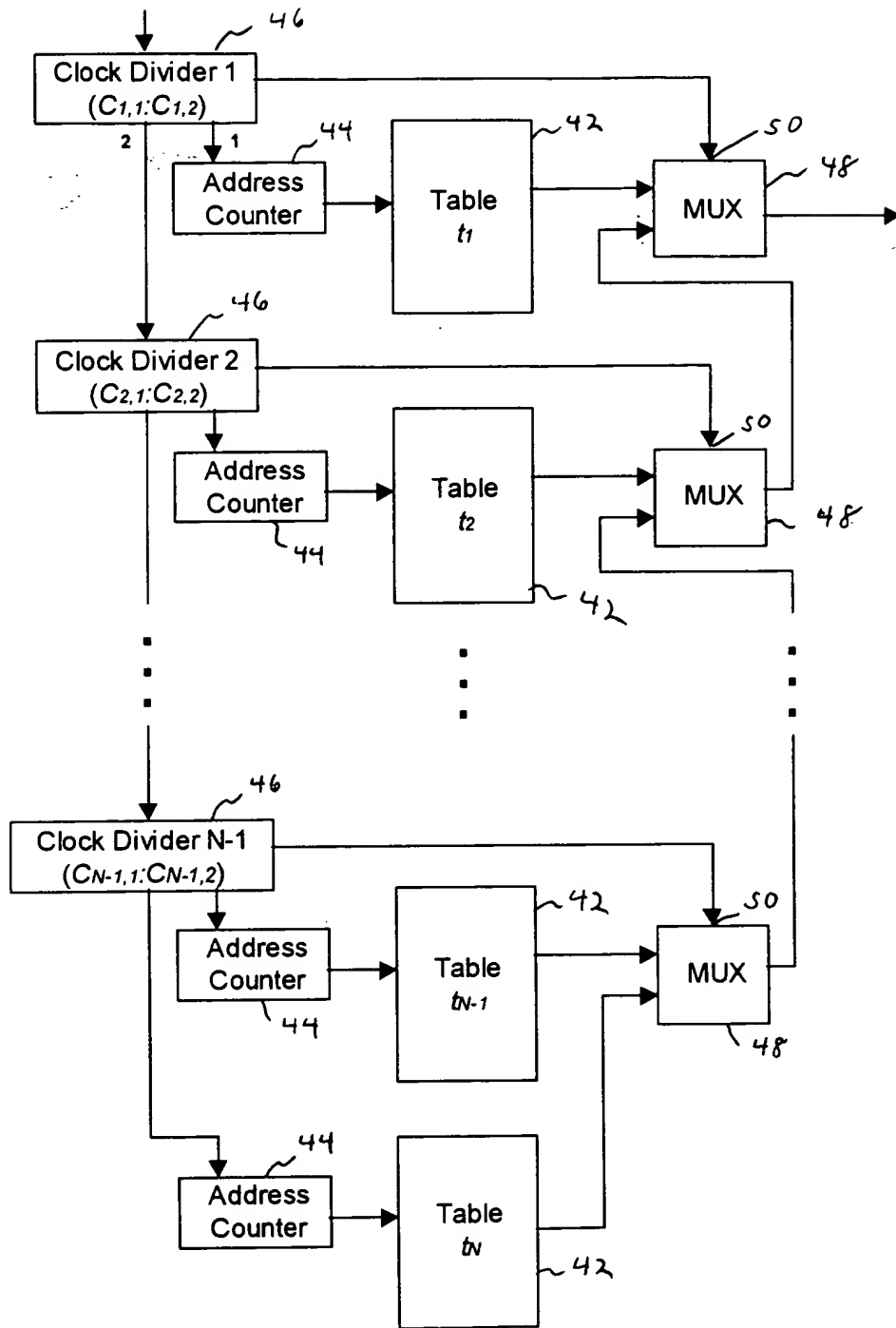


Figure 4. Recursive implementation of grant generator using multi-tables.

Fig. 5A

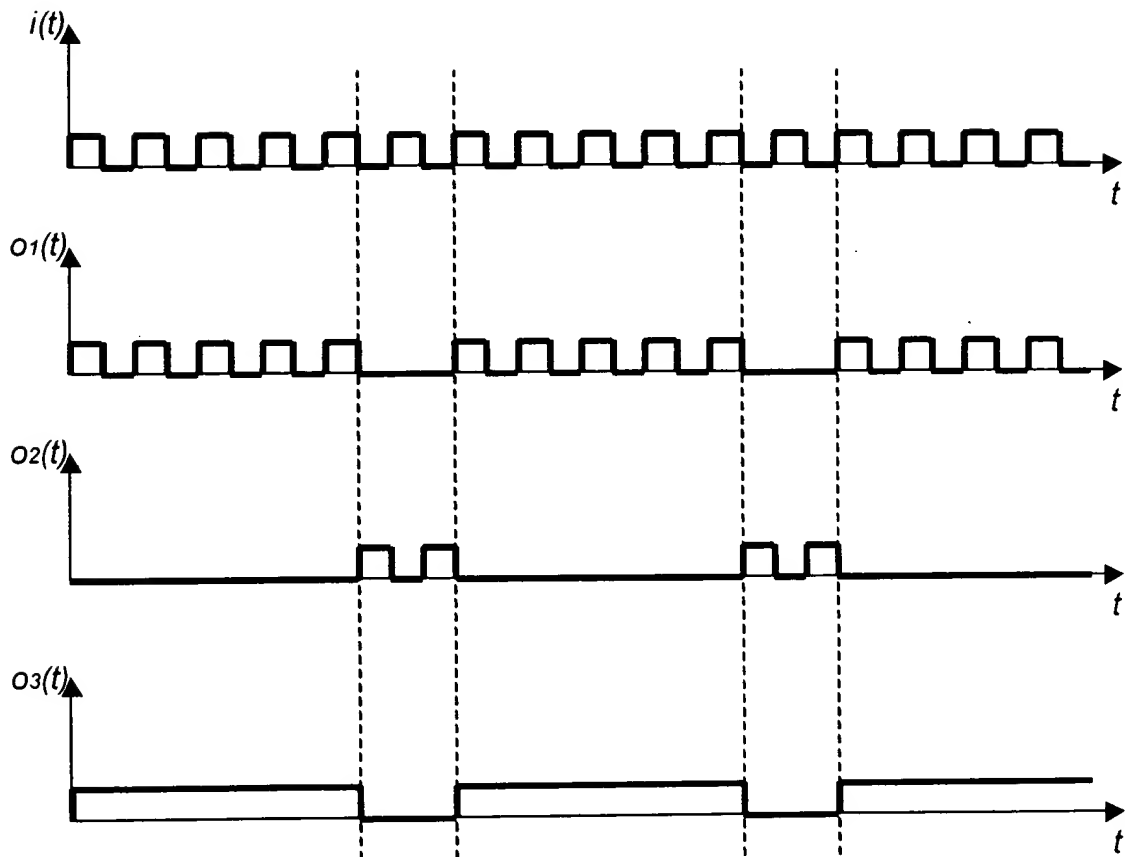
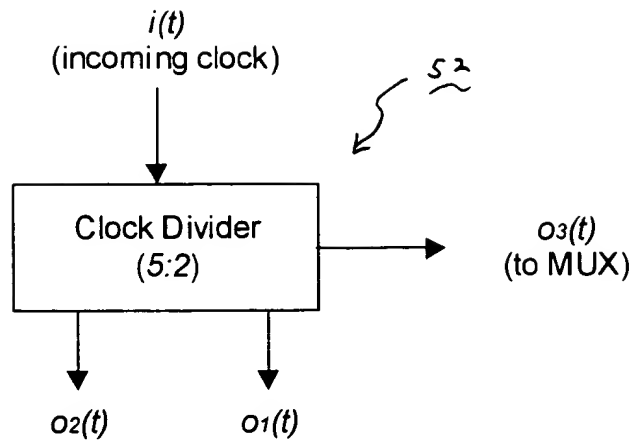


Figure 5B Example timing diagram for input and output signals of clock divider with division ratio 5:2.

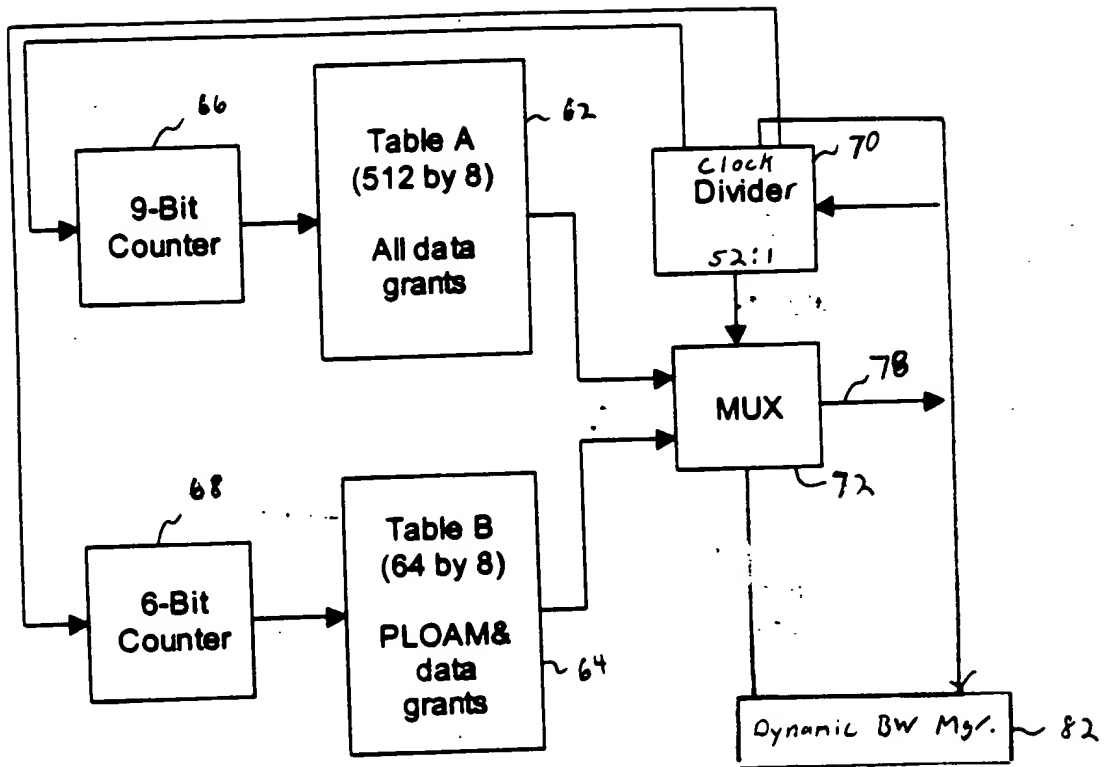


Fig 7

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